Sub D1

1. (Twice Amended) A semiconductor structure comprising:

an insulator layer;

a conductive plug positioned within said insulator layer and formed of a single conductive material;

a doped region connected to said conductive plug;

an etch-stop layer located on said insulator layer and surrounding said plug;

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a non-conductive layer having an etched via at least partially over said conductive plug; and

a conductive connector formed in said via in electrical contact with said plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over and in contact with said first conductive layer, said first conductive layer including a portion in contact with said conductive plug.

Sub C1

B2 Cont

11. (Amended) A semiconductor device comprising:

at least one memory cell comprising:

an active region in a substrate;

a conductive plug positioned within an insulator layer and provided over said active region, said conductive plug being electrically connected with said active region;

an etch-stop layer deposited on said insulator and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer and having at least a first and a second etched via over said plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

at least one conductive layer in said first and second vias in electrical connection with said plug.

18. (Twice Amended) A semiconductor device comprising:

a conductive element formed of a single conductive material;

an etch-resistant layer surrounding an upper portion of said conductive element;

a non-conductive layer over said etch resistant layer and having a via over said conductive element, said via extending down to a level of said conductive element and etch resistant layer;

a conductive material located in said via, wherein said conductive material in said via contacts said conductive element; and

a doped region connected to said conductive element.

25. (Amended) A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a conductive plug positioned within an insulator and provided on a connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via over said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and second etched vias, said first conductive layer including a portion in contact with said conductive plug.